FIG.1

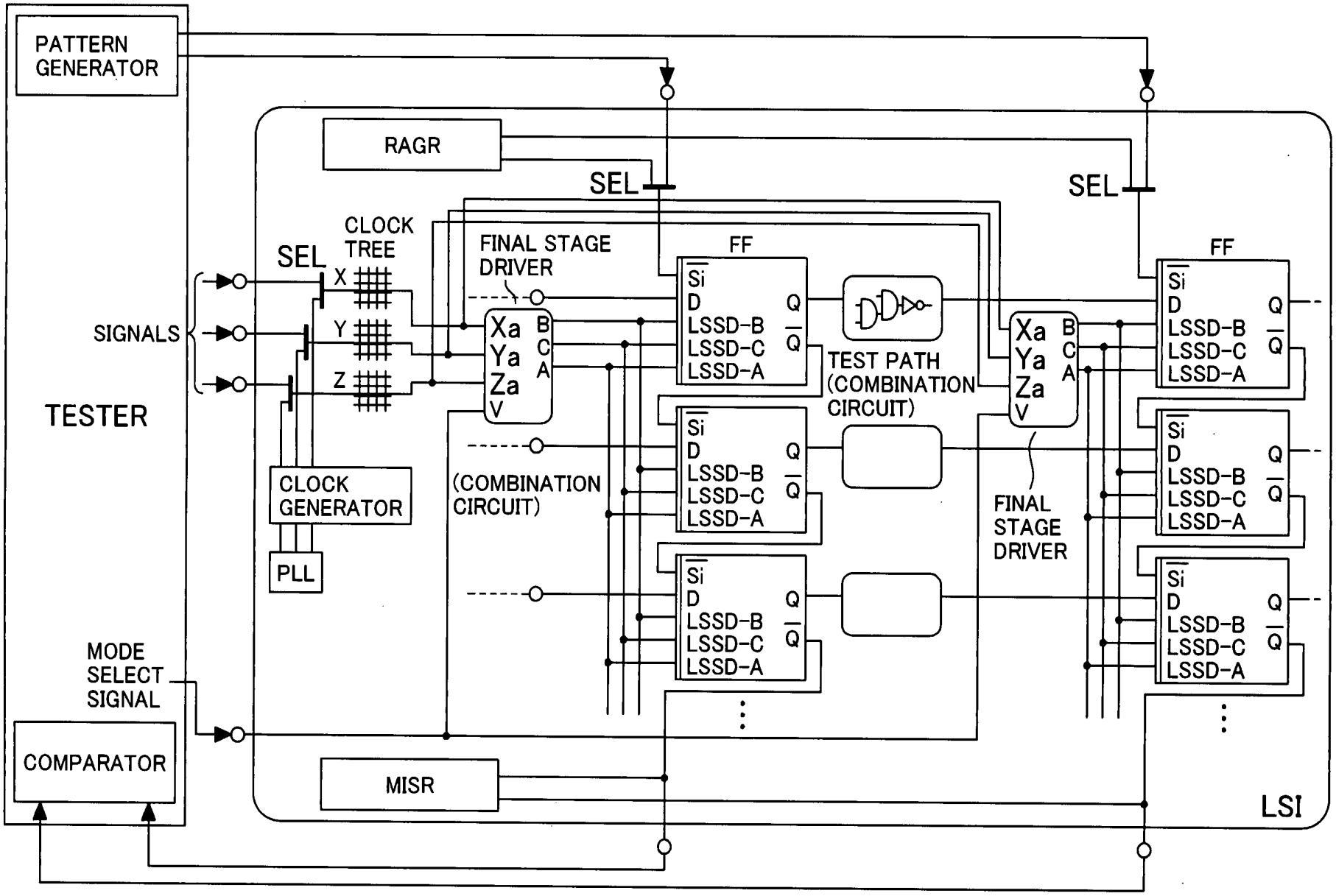

PATTERN GENERATOR
RAGR
SEL
SEL
CLOCK TREE
SEL
X
Y
Z
FINAL STAGE DRIVER
FF
FF
SIGNALS
TESTER
Xa
Ya
Za
V
B
C
A
Si
D
LSSD-B
LSSD-C
LSSD-A
Q
TEST PATH (COMBINATION CIRCUIT)
(COMBINATION CIRCUIT)
FINAL STAGE DRIVER
CLOCK GENERATOR
PLL
MODE SELECT SIGNAL
COMPARATOR
MISR
LSI

FIG.2

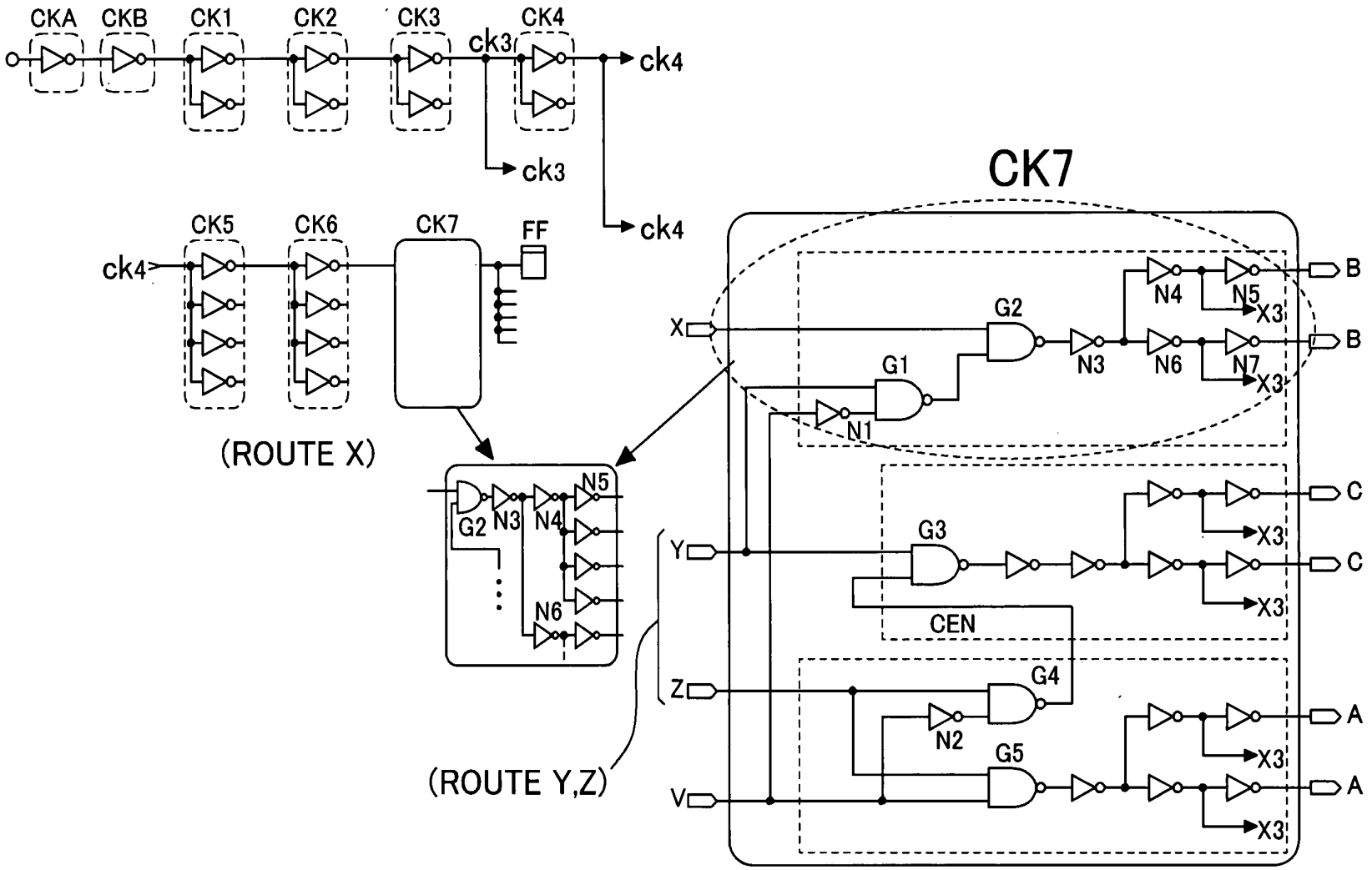

CKA
CKB
CK1
CK2
CK3
CK4
ck3
ck4
ck3
ck4
CK5
CK6
CK7
FF
ck4
(ROUTE X)
CK7
X
Y
Z
V
G1
G2
G3
G4
G5
N1
N2
N3
N4
N5
N6
N7
X3
B
C
A
CEN
(ROUTE Y,Z)

FIG.3

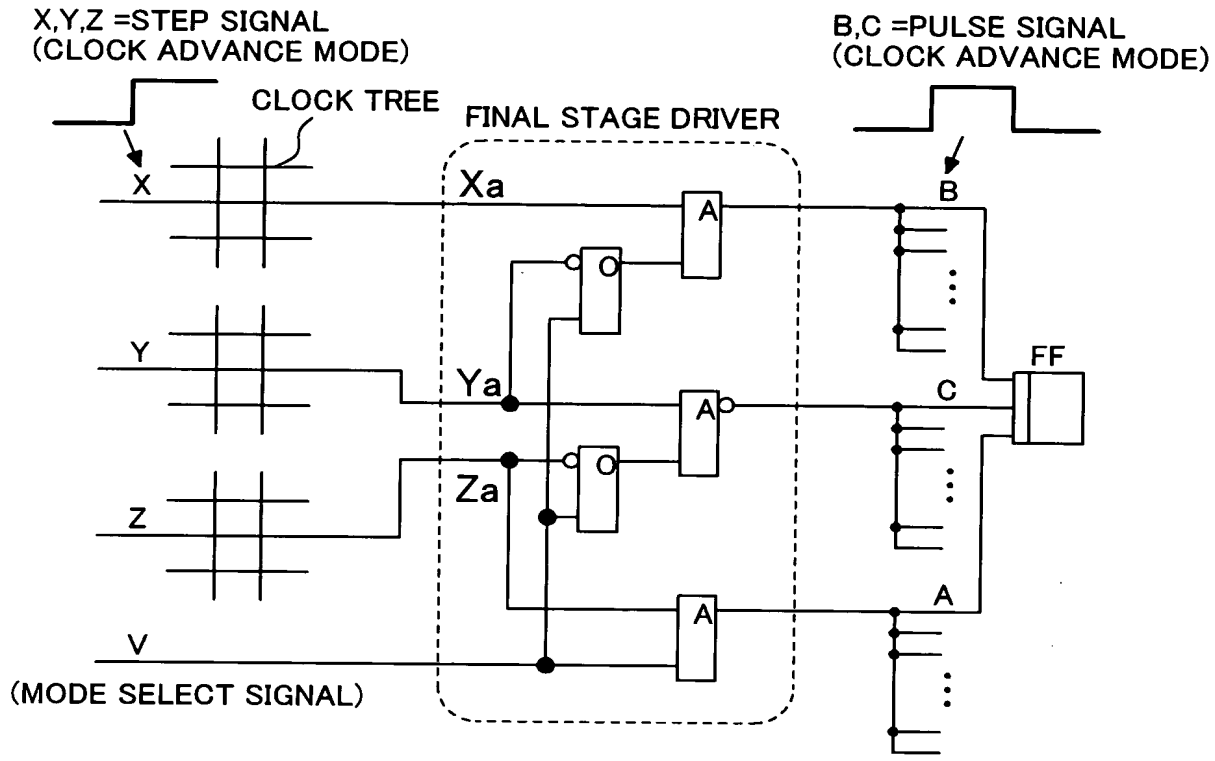

X,Y,Z =STEP SIGNAL
(CLOCK ADVANCE MODE)
B,C =PULSE SIGNAL
(CLOCK ADVANCE MODE)
CLOCK TREE
FINAL STAGE DRIVER
X
Y
Z
V
(MODE SELECT SIGNAL)
Xa
Ya
Za
A
O
B
C
FF

FIG.4

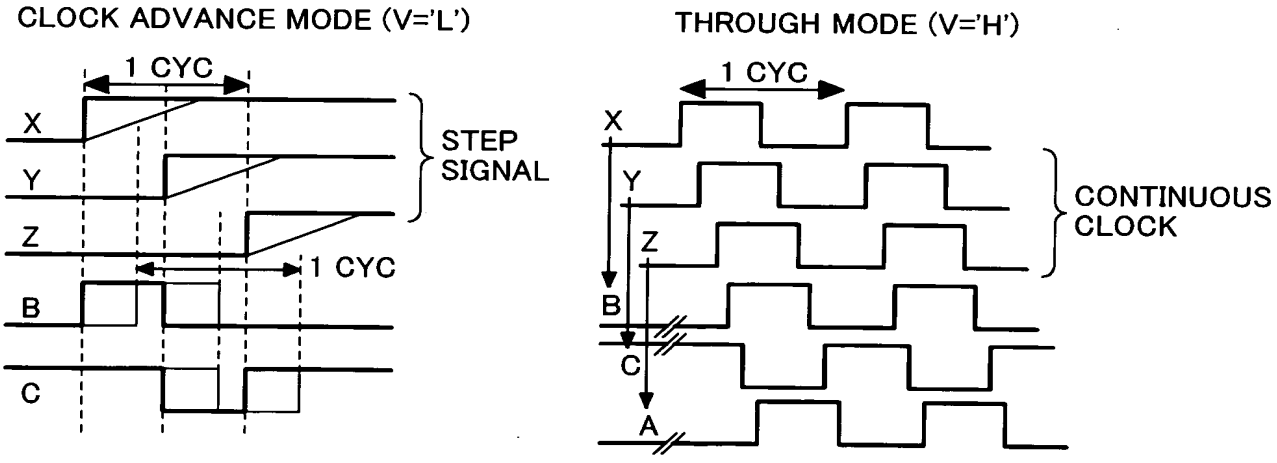

CLOCK ADVANCE MODE (V='L')
1 CYC
X
Y
Z
STEP
SIGNAL
1 CYC
B
C
THROUGH MODE (V='H')
1 CYC
X
Y
Z
B
C
A
CONTINUOUS
CLOCK

FIG.5

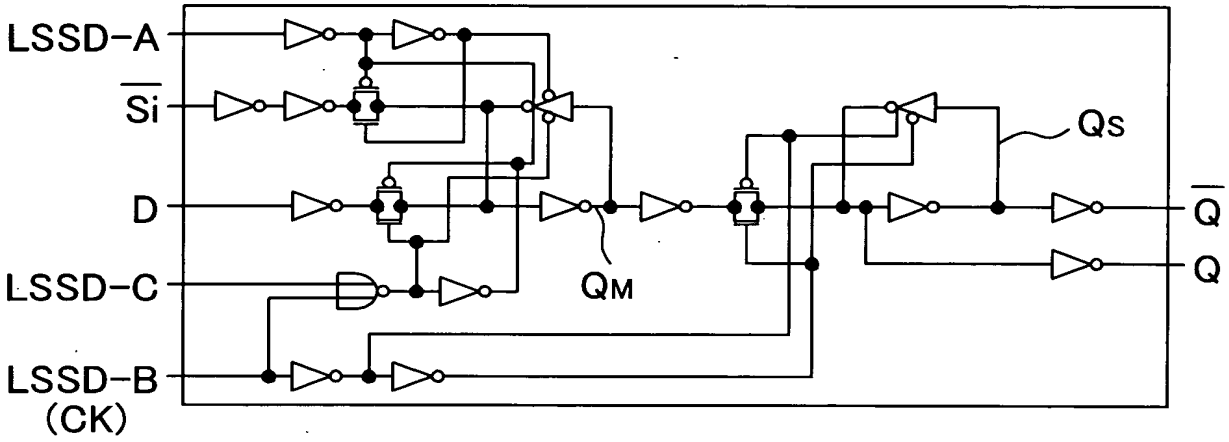


FIG.6

INPUT					INTERMEDIATE NODE		OUTPUT		NOTE
CK	D	LSSD-A	LSSD-C	$\overline{Si}$	QM	QS	Q	$\overline{Q}$	
L	*	L	L	*	D	QS−1	QS	$\overline{QS}$	NORMAL
H	*	L	L	*	QM−1	QM	QS	$\overline{QS}$	NORMAL
⎍	L	L	L	*	L	QM	L	H	NORMAL
⎍	H	L	L	*	H	QM	H	L	NORMAL
L	*	L	H	*	QM−1	QS−1	QS	$\overline{QS}$	DIAGNOSTIC
H	*	L	H	*	QM−1	QM	QS	$\overline{QS}$	DIAGNOSTIC
L	*	H	H	L	H	QS−1	QS	$\overline{QS}$	DIAGNOSTIC
L	*	H	H	H	L	QS−1	QS	$\overline{QS}$	DIAGNOSTIC
*	*	H	L	*					PROHIBITED
H	*	H	H	*					PROHIBITED

FIG.7

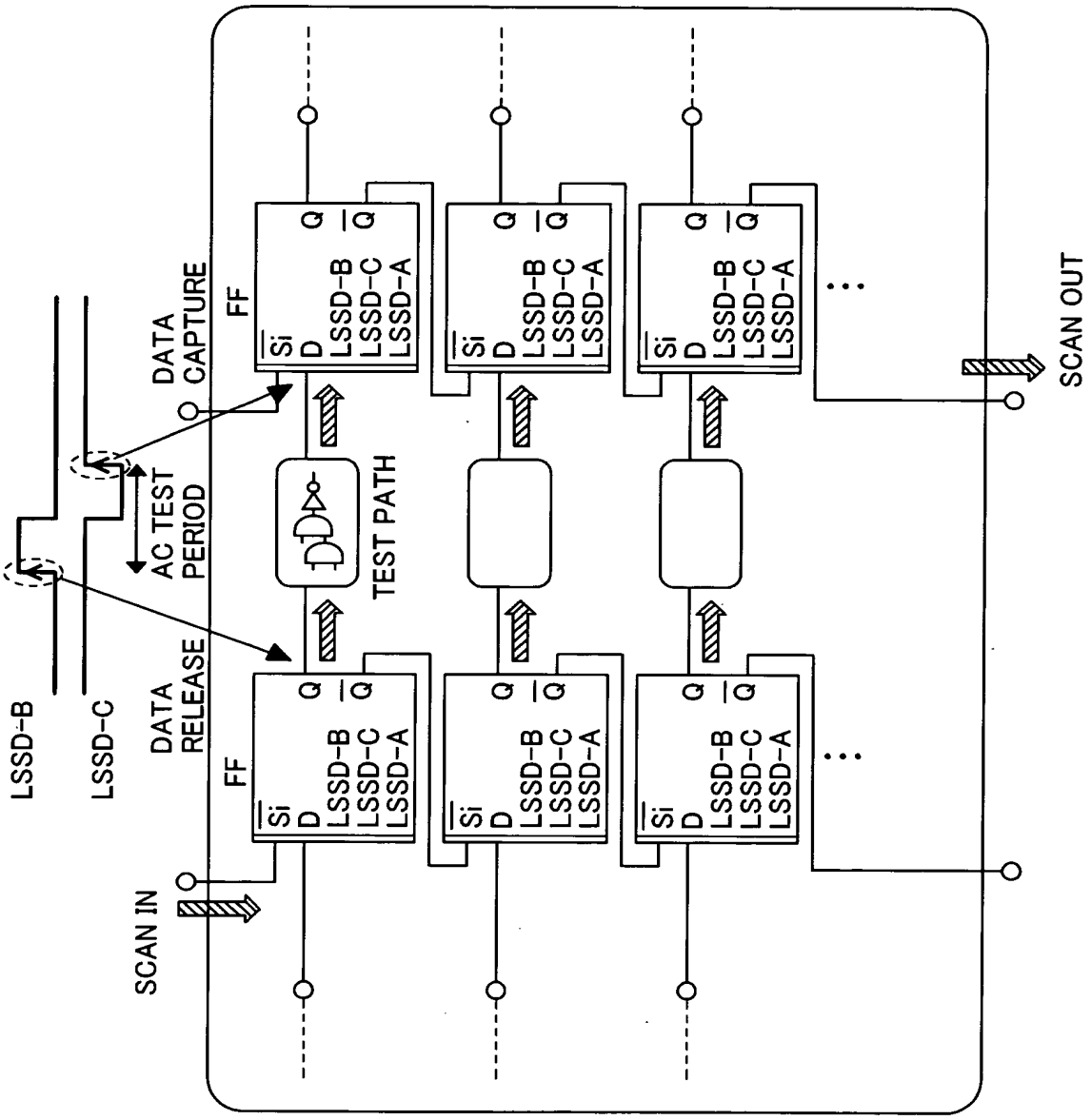

LSSD-B
LSSD-C
DATA RELEASE
DATA CAPTURE
AC TEST PERIOD
TEST PATH
SCAN IN
SCAN OUT
FF
Si
D
Q
LSSD-B
LSSD-C
LSSD-A

FIG.8A FIG.8B FIG.8C FIG.8D

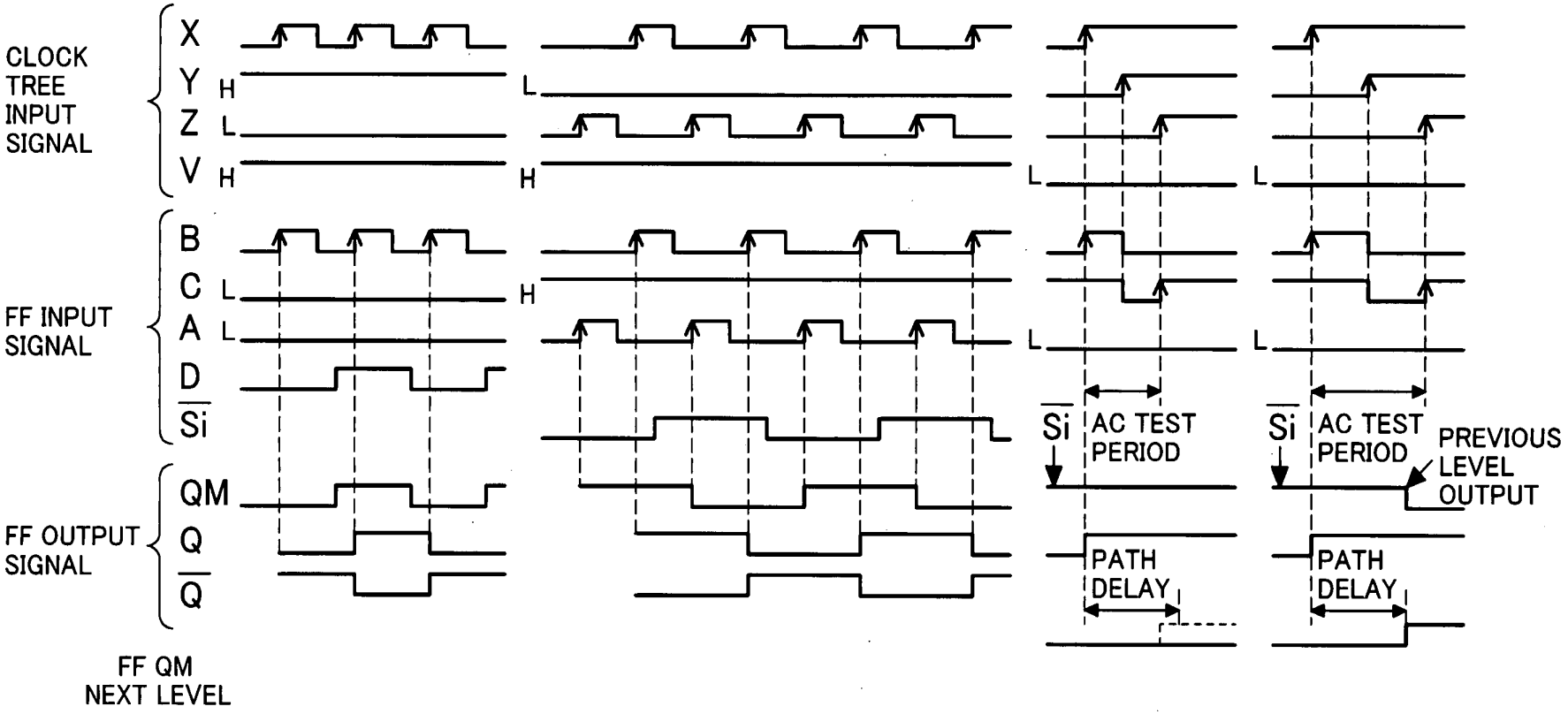


FIG.9

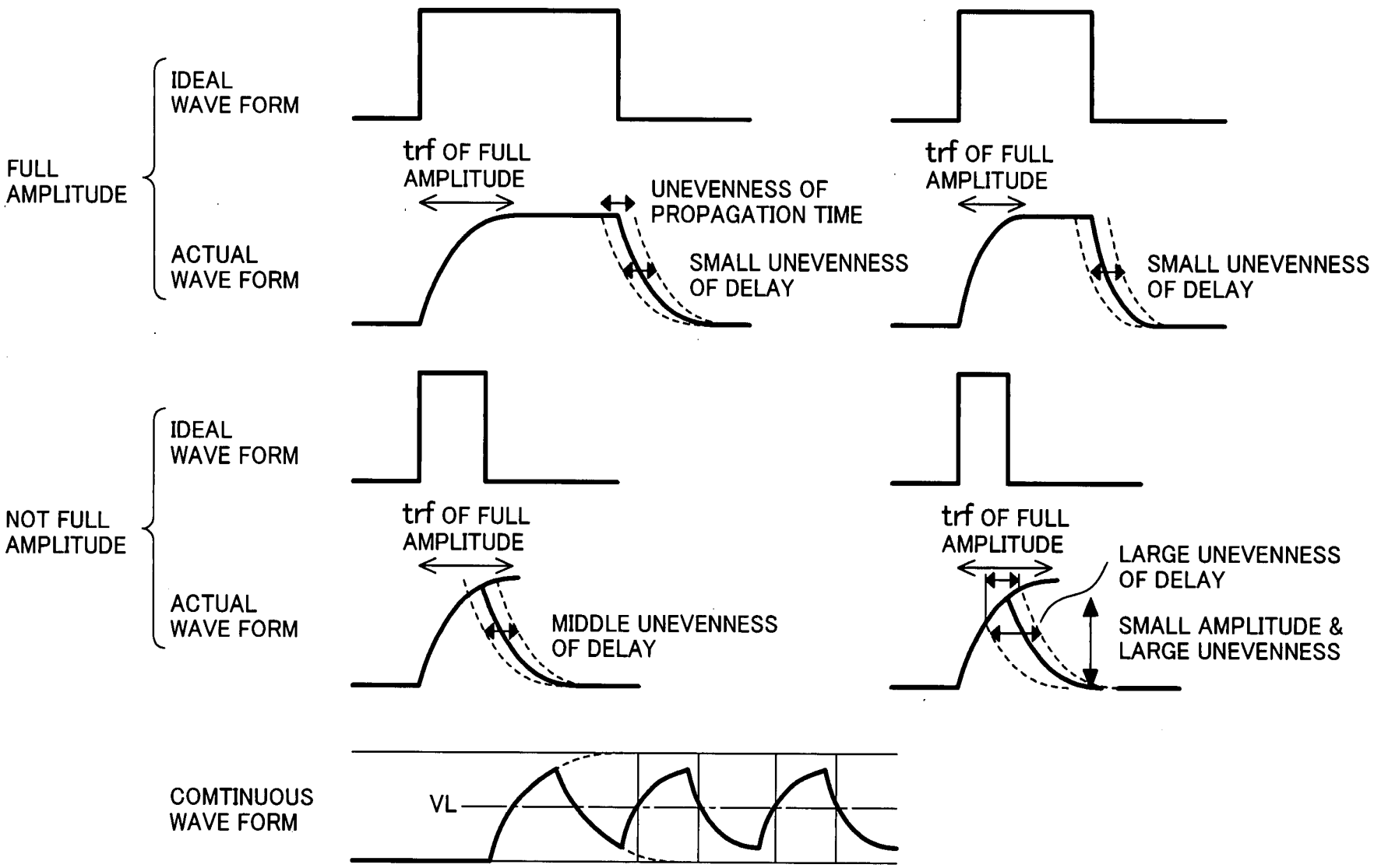

FULL AMPLITUDE
IDEAL WAVE FORM
ACTUAL WAVE FORM
trf OF FULL AMPLITUDE
UNEVENNESS OF PROPAGATION TIME
SMALL UNEVENNESS OF DELAY
trf OF FULL AMPLITUDE
SMALL UNEVENNESS OF DELAY
NOT FULL AMPLITUDE
IDEAL WAVE FORM
ACTUAL WAVE FORM
trf OF FULL AMPLITUDE
MIDDLE UNEVENNESS OF DELAY
trf OF FULL AMPLITUDE
LARGE UNEVENNESS OF DELAY
SMALL AMPLITUDE & LARGE UNEVENNESS
COMTINUOUS WAVE FORM
VL

FIG.10

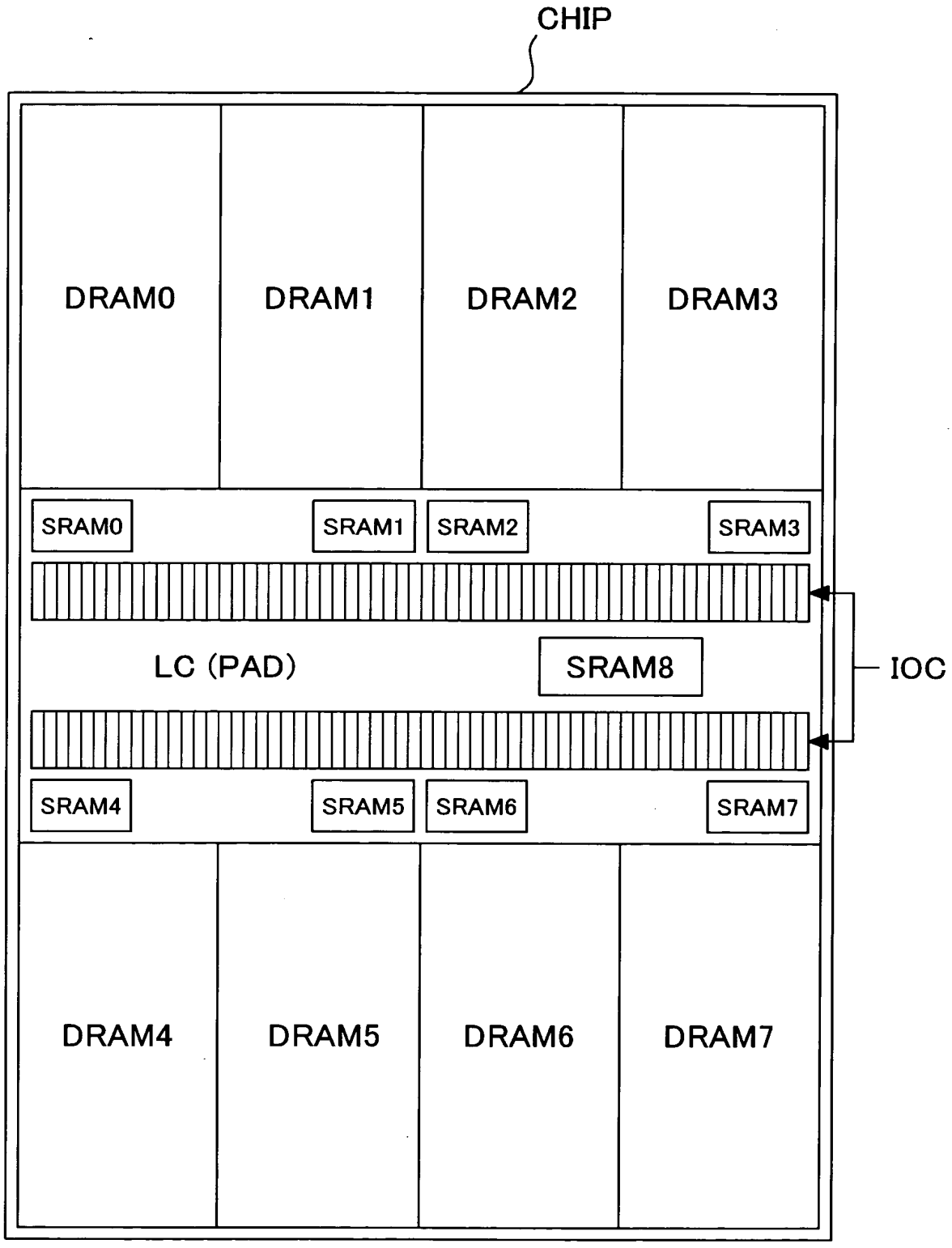

CHIP
DRAM0
DRAM1
DRAM2
DRAM3
SRAM0
SRAM1
SRAM2
SRAM3
LC (PAD)
SRAM8
IOC
SRAM4
SRAM5
SRAM6
SRAM7
DRAM4
DRAM5
DRAM6
DRAM7

FIG.11

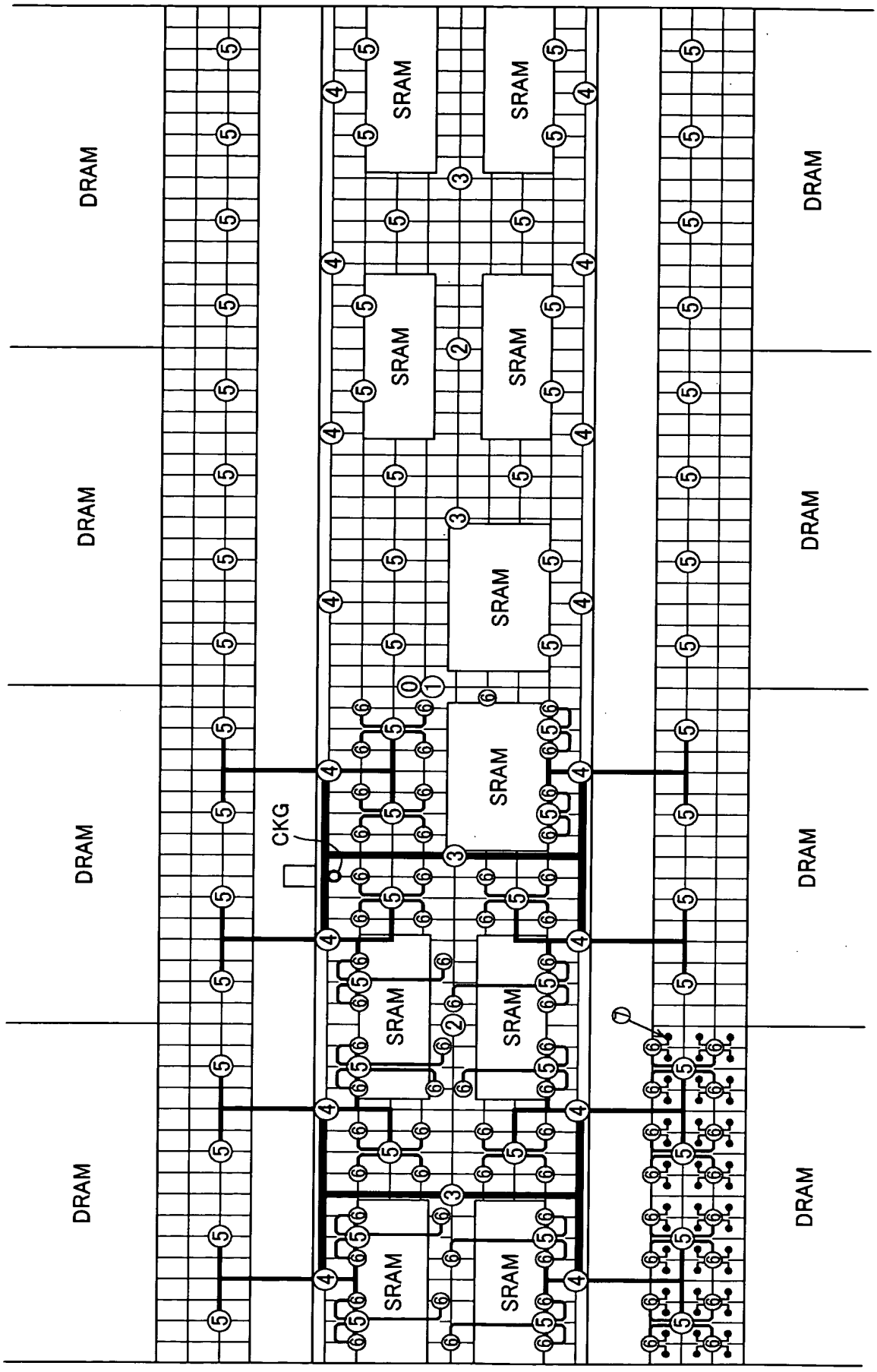

DRAM
DRAM
DRAM
DRAM
DRAM
DRAM
SRAM
SRAM
SRAM
SRAM
SRAM
SRAM
SRAM
SRAM
CKG

FIG.12

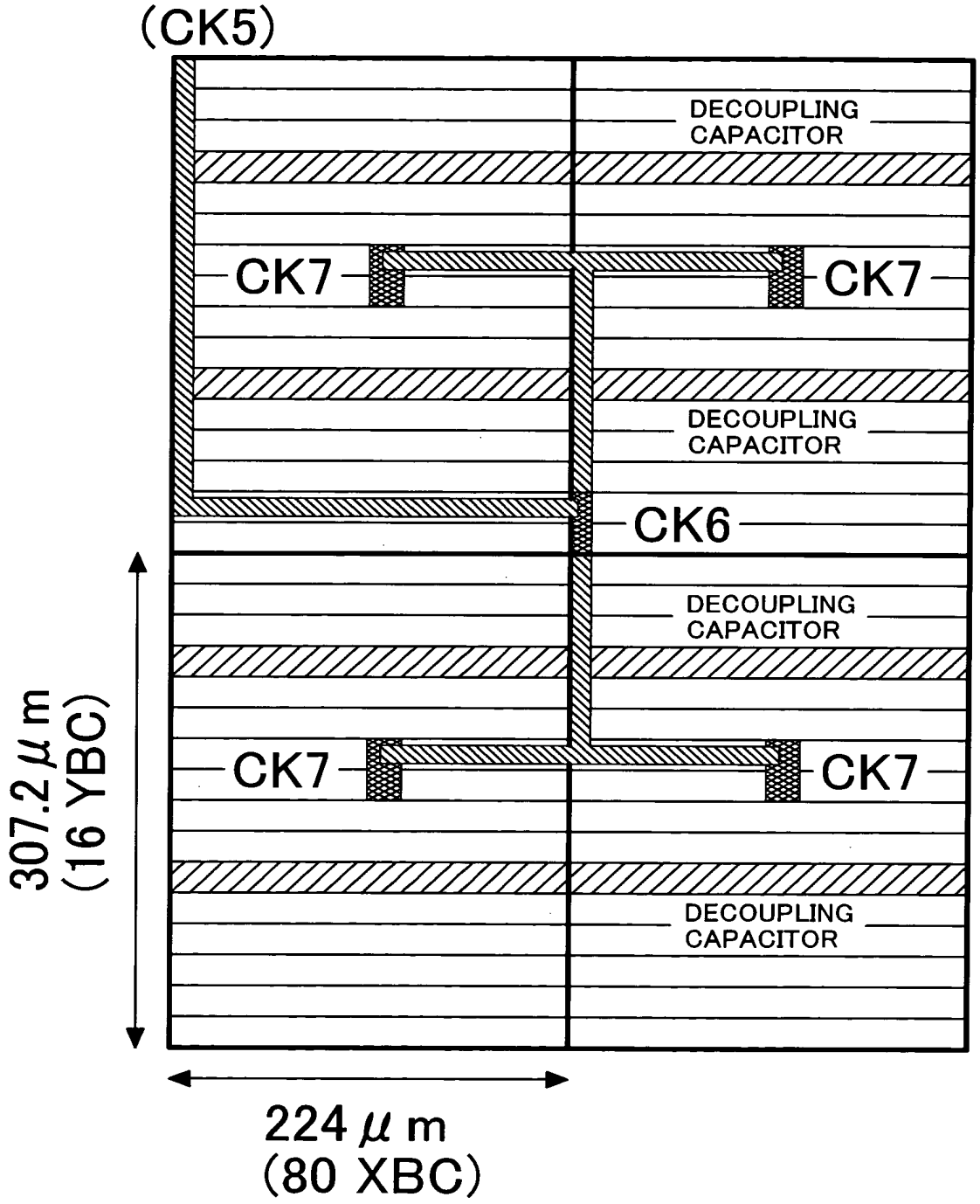
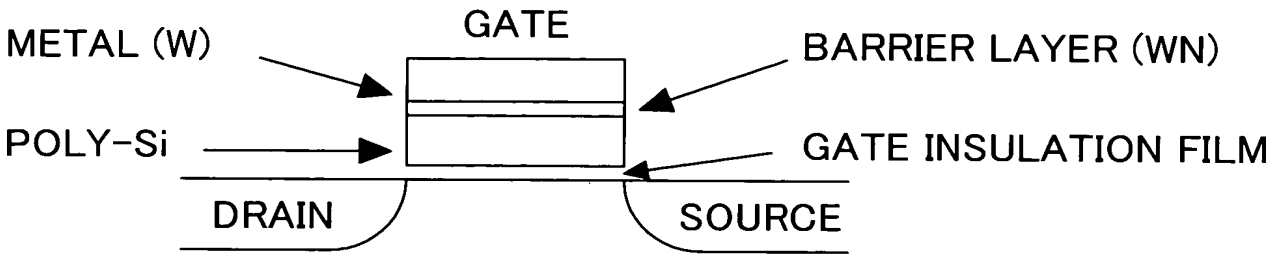

(CK5)
DECOUPLING CAPACITOR
CK7
CK7
DECOUPLING CAPACITOR
CK6
DECOUPLING CAPACITOR
CK7
CK7
DECOUPLING CAPACITOR
307.2 μm (16 YBC)
224 μm (80 XBC)

FIG.13


METAL (W)
GATE
BARRIER LAYER (WN)
POLY-Si
GATE INSULATION FILM
DRAIN
SOURCE